What is claimed is:

1. A semiconductor integrated circuit device including:

a first electrode for an information storage capacitance device, disposed for each memory cell;

a second electrode so formed as to oppose said first electrode;

a capacitance insulating film formed between said first and second electrodes;

a wire formed over said second electrode; and

a connection member for connecting electrically said wire and said second electrode;

wherein:

said connection member contains a titanium layer or a titanium nitride layer;

said second electrode contains a first layer formed on the side of said capacitance insulating film and a second layer formed on the side of said wire; and

said first layer is a metal film formed by oxygen-containing chemical vapor phase growth, and not containing oxygen.

2. A semiconductor integrated circuit device according to claim 1, wherein said second layer is a tungsten layer.

3. A semiconductor integrated circuit device according to claim 2, wherein said tungsten layer contains a first tungsten layer formed by sputtering and a second tungsten layer formed by chemical vapor phase growth.

4. A semiconductor integrated circuit device including:

a first electrode for an information storage capacitance device, disposed for each memory cell;

a second electrode so formed as to oppose said first electrode;

a capacitance insulating film formed between said first and second electrodes; and

an insulating film covering said second electrode;

said capacitance insulating film comprising a high dielectric layer or a ferroelectric layer; wherein:

said second electrode contains a first layer formed on the side of said capacitance insulating film and an electrically conductive second layer formed on said first layer; and

said second layer is made of a material having a lower etching rate than a material constituting said first layer under the etching condition of said

insulating film.

5. A semiconductor integrated circuit device including:

a first electrode for an information storage capacitance device, disposed for each memory cell;

a second electrode so formed as to oppose said first electrode; and

a capacitance insulating film formed between said first and second electrodes;

said capacitance film comprising a high dielectric layer or a ferroelectric layer;

wherein:

said second electrode contains a first layer formed on the side of said capacitance and a second layer formed over said first layer; and

said second layer is made of a material having a lower evaporation rate in an oxidizing atmosphere than that of a material constituting said first layer.

6. A semiconductor integrated circuit device including:

a first electrode for an information storage capacitance device, disposed for each memory cell;

a second electrode so formed as to oppose said first electrode; and

a capacitance insulating film formed between

said first and second electrodes;

said capacitance insulating film comprising a high dielectric layer or a ferroelectric layer;

wherein:

said second electrode contains a first layer formed on the side of said capacitance insulating film and a second layer formed over said first layer; and

the film thickness of said second layer is greater than that of said first layer.

7. A semiconductor integrated circuit device according to claim 6, wherein resistivity of said second layer is smaller than that of said first layer.

8. A semiconductor integrated circuit device according to claim 7, wherein an internal stress of said second electrode is smaller than an internal stress when said second electrode is made of a material constituting said first layer.

9. A semiconductor integrated circuit device including:

a first electrode for an information storage capacitance device, disposed for each memory cell;

a second electrode so formed as to oppose said first electrode; and

a capacitance insulating film formed between said first and second electrodes;

said capacitance insulating film comprising a high dielectric layer or a ferroelectric layer;

wherein:

said second electrode contains a first layer formed on the side of said capacitance insulating film and a second layer formed over said first layer; and

an angle between a taper surface and a base in a processed section, when a material of said second layer is processed by anisotropic dry etching, is greater than an angle between the taper surface and the base in a processing section of a material of said first layer under the same etching condition.

10. A semiconductor integrated circuit device including:

a first electrode for an information storage capacitance device, disposed for each memory cell;

a second electrode so formed as to oppose said first electrode; and

a capacitance insulating film formed between said first and second electrodes;

said capacitance insulating film comprising a high dielectric layer or a ferroelectric layer;

wherein:

said second electrode contains a first layer formed on the side of said capacitance insulating film

and a second layer formed over said first layer; and

the sectional shape at the edge portion of each of said first and second layers is processed into a taper shape.

11. A semiconductor integrated circuit device according to claim 10, wherein said sectional shape is such that the distance from the leg of the vertical drawn from the upper end of said tapered processing surface to the surface of the base to the lower end of said taper surface is at least 1/2 of a minimum processing size.

12. A semiconductor integrated circuit device including:

a first electrode for an information storage capacitance device, disposed for each memory cell;

a second electrode so formed as to oppose said first electrode; and

a capacitance insulating film formed between said first and second electrodes;

said capacitance insulating film comprising a high dielectric layer or a ferroelectric layer;

said first electrode being shaped into a columnar or cylindrical cubic shape;

wherein:

said second electrode contains a first layer

formed on the side of said capacitance insulating film and a second layer formed over said first layer;

a film thickness T1 of said first layer satisfies the condition T1 > (d - 2 x Tins)/2; and

a film thickness T2 of said second layer satisfies the condition T2 > T1; where d is the distance between said first electrodes adjacent to each other or an inner diameter of the cylindrical shape of said first electrode, and Tins is the film thickness of said capacitance insulating film.

13. A semiconductor integrated circuit device according to claim 6, wherein said first layer is a film of precious metals, their silicide or oxide film, or their compound film.

14. A semiconductor integrated circuit device according to claim 13, wherein said first layer is a platinum film, a ruthenium film, a ruthenium silicide film or an SRO ($SrRuO_x$) film.

15. A semiconductor integrated circuit device according to claim 14, wherein said capacitance insulating film is a BST ($Ba_xSr_{1-x}TiO_3$) film, an STO ($SrTiO_3$) film or a tantalum oxide (Ta_2O_5) film.

16. A semiconductor integrated circuit device according to claim 14, wherein said first layer is a titanium nitride film and said capacitance insulating

film is a tantalum oxide (Ta_2O_5) film.

17. A semiconductor integrated circuit device according to claim 14, wherein said second layer is a metal film of an element belonging to the Groups IVb, Vb or VIb, or its silicide or compound film.

18. A semiconductor integrated circuit device according to claim 17, wherein said second layer is a tungsten (W) film, a titanium (Ti) film, a tantalum (Ta) film, a tungsten nitride (WN) film, a titanium nitride (TiN) film, a tantalum nitride (TaN) film, a titanium aluminum nitride (TiAlN) film, a titanium silicon nitride (TiSiN) film, a tungsten silicon nitride (WSiN) film or a tantalum silicon nitride (TaSiN) film.

19. A semiconductor integrated circuit device according to claim 17, which further includes a third layer comprising a titanium nitride film, a titanium silicon nitride film or a titanium compound film in addition to said first and second layers.

20. A method of producing a semiconductor integrated circuit device comprising the steps of:

(a) forming bit lines and a first layer wiring over MISFET on a main plane of a semiconductor substrate through a first inter-layer insulating film, forming a second inter-layer insulating film and an

electrode-forming insulating film, and boring holes in said electrode-forming insulating film;

(b) forming a metal or a metal compound for burying the inside of said holes, and then forming columnar or cylindrical first electrodes by removing said electrode-forming insulating film or by forming a metal film or a metal compound film covering the inner wall of said holes;

(c) depositing a ferroelectric or high dielectric capacitance insulating film to cover said first electrode, and depositing further a first conductor layer and a second conductor layer;

(d) patterning said first and second conductor layers to form second electrodes; and

(e) depositing a third inter-layer insulating film covering said second electrodes, and forming first connection holes reaching said second electrode and second connection holes reaching said first layer wiring, by etching.

21. A method of producing a semiconductor integrated circuit device according to claim 20, wherein, after said second layer is etched in said etching step of said second electrode, said first layer is etched by using said second layer, that is patterned, as a mask.

22. A method of producing a semiconductor integrated

circuit device including the steps of:

(a) forming first electrodes on a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrode;

(c) forming second electrodes over said capacitance insulating film;

(d) forming a second insulating film having an opening for exposing a part of said second electrode, on said second electrode; and

(e) forming a first conductor layer inside said opening; wherein:

the formation step of said second electrode includes the steps of:

(i) forming a first metal layer by a chemical vapor phase growing method containing oxygen over said capacitance insulating film; and

(ii) forming a second metal layer not containing oxygen over said first metal layer.

23. A method of producing a semiconductor integrated circuit device according to claim 22, wherein said first metal layer is a platinum film or a ruthenium film.

24. A method of producing a semiconductor integrated

circuit device according to claim 22, wherein said second metal layer comprises a tungsten film or a tungsten nitride film.

Sub D1

25. A method of producing a semiconductor integrated circuit device according to claim 22, wherein said second metal layer is formed by a sputtering method.

Sub D2

26. A method of producing a semiconductor integrated circuit device including the steps of:

(a) forming a plurality of mutually spaced-part first electrodes over a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrodes; and

(c) forming continuously second electrodes with respect to a plurality of said first electrodes, over said capacitance insulating film; wherein:

the formation step of said second electrodes includes the steps of:

(i) forming a first metal layer over said capacitance insulating film; and

(ii) forming a second metal layer having a greater film thickness than said first metal layer over said first metal layer.

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27. A method of producing a semiconductor integrated circuit device according to claim 26, wherein

resistivity of said second metal layer is smaller than that of said first metal layer.

28. A method of producing a semiconductor integrated circuit device according to claim 27, wherein said first metal layer is a platinum film or a ruthenium film, and said second metal layer is a tungsten film or a tungsten nitride film.

29. A method of producing a semiconductor integrated circuit device including the steps of:

(a) forming a plurality of mutually spaced-apart first electrodes over a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrodes; and

(c) forming continuously second electrodes with respect to a plurality of said first electrodes, over said capacitance insulating film; wherein:

the formation step of said second electrodes includes the steps of:

(i) forming a first metal layer over said capacitance insulating film in such a fashion as to bury the spaces between said mutually spaced-apart first electrodes; and

(ii) forming said second metal layer over said first metal layer.

30. A method of producing a semiconductor integrated circuit device according to claim 29, wherein said second metal layer is formed by a sputtering method.

31. A method of producing a semiconductor integrated circuit device according to claim 29, wherein said second metal layer comprises a third metal layer formed by a sputtering method and a fourth metal layer formed by a chemical vapor phase growing method over said third metal layer.

32. A method of producing a semiconductor integrated circuit device according to claim 29, wherein the film thickness of said second metal layer is greater than that of said first metal layer.

33. A method of producing a semiconductor integrated circuit device according to claim 29, wherein said first metal layer is a platinum film or a ruthenium film, and said second metal layer is a tungsten film or a tungsten nitride film.